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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/815,594	03/23/2001	Yasuhiro Yoshida	55707(904)	7185
21874	7590	06/29/2005	EXAMINER	
EDWARDS & ANGELL, LLP P.O. BOX 55874 BOSTON, MA 02205			GOOD JOHNSON, MOTILEWA	
			ART UNIT	PAPER NUMBER
			2677	

DATE MAILED: 06/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/815,594

Applicant(s)

YOSHIDA ET AL.

Examiner

Motilewa A. Good-Johnson

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 26 April 2005.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-62 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-8, 10-18, 20-22, 26-34, 38-46, 48-50 and 52-64 is/are rejected.
- 7) ☒ Claim(s) 9, 19, 23-25, 35-37, 47, 51 and 55 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 04/26/2005.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-8, 10-18, 20-22, 26-34, 38-46, 48-50 and 52-54 are rejected under 35 U.S.C. 103(a) as being unpatentable over Clatanoff et al., U.S. Patent Number 6,052,491, in view of Pettitt, U.S. Patent Number 6,040,876.

Regarding claim 1, Clatanoff discloses a first signal processing circuit (figure 14, element 308) for applying gamma correction to an n-bit digital signal inputted as a video signal (col. 6, lines 4-5), and for converting the digital signal into an m-bit digital signal (col. 6, lines 5-6); and a second signal processing circuit (figure 14, element 1404); outputting a truncated integer portion of the resulting output m-bit digital signal (col. 6, lines 4-17)

However it is noted that Clatanoff fails to disclose for adding a noise signal to the m-bit digital signal.

Pettitt discloses a first signal processing circuit for applying gamma correction (112) to an n-bit digital signal inputted as a video signal, and for converting the digital signal into an m-bit digital signal (figure 4, col. 4, lines 15-20); and a second signal

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processing circuit for adding a noise signal (figure 5, col. 4, lines 38-42) to the m-bit digital signal from said first signal processing circuit, and for outputting a Q-bit digital signal obtained from rounding down a less significant (m-Q) bit from the m-bit digital signal (col. 4, lines 20-25)

It would have been obvious to one of ordinary skill in the art at the time of the invention to include in the dither circuit as disclosed in Clatanoff, the random noise generated as disclosed in Pettitt, to reduce the effects of false contouring for a digital signal.

Regarding claim 2, Pettitt discloses first signal processing circuit includes bit-converting means for converting the inputted n-bit digital signal into the m-bit digital signal in accordance with a pre-set value (col. 3, lines 49-58)

Regarding claim 3, Pettitt discloses bit-converting means is a look up table, which outputs the m-bit digital signal that is the present value in accordance with the inputted n-bit digital signal (col. 3, lines 28-30)

Regarding claim 4, Clatanoff discloses said bit converting means is a calculating device for converting the n-bit digital signal into the m-bit . . . digital signal by numerical calculation (col. 6, lines 55-67)

Regarding claim 5, Pettitt discloses said first signal processing circuit and said second signal processing circuit are provided for respective RGB colors (col. 3, lines 21-22)

Regarding claim 6, Pettitt discloses an average value of a signal level is set to zero (table 3)

Regarding claim 7, Pettitt discloses the noise signal is a random noise signal with no regularity in its cycle of amplitude (col. 4, line 45)

Regarding claim 8, Pettitt discloses the noise signal is obtained from, by using an arbitrary noise pattern table, switching a starting point of the noise pattern table per field or per noise pattern table (table 3)

Regarding claim 10, it is rejected based upon similar rational as claim 1. Further, Pettitt discloses an image processing apparatus, comprising: a signal processing circuit for adding a noise signal (figure 5, col. 4, lines 38-53) to an inputted m-bit digital signal, and for outputting a Q-bit digital signal obtained from rounding off a less significant bit from the m-bit digital signal (col. 4, lines 15-24)

Regarding claim 11, Pettitt discloses display means (114) for displaying an image; and Clatanoff discloses driving means for driving the display means (col. 4, lines 7-42)

Regarding claim 12, it is rejected based upon similar rational as above dependent claim 2.

Regarding claim 13, Clatanoff discloses the pre-set value in said bit converting means is rewritable so that unevenness in properties of said driving means may be absorbed (col. 8, lines 1-5)

Regarding claim 14, Clatanoff discloses the pre-set value in said bit converting means is rewritten in accordance with brightness in surrounding of said image display apparatus (col. 8, lines 1-19)

Regarding claim 15, Clatanoff discloses the pre-set value in said bit converting means is rewritten in accordance with brightness of overall display image of said display means (col. 8, lines 1-19)

Regarding claim 16, it is rejected based upon similar rational as claim 10.

Regarding claim 17, it is rejected based similar rational as claim 1.

Regarding claim 18, Pettitt discloses second signal processing circuit includes: a noise generating circuit . . . (figure 5); an adding circuit for adding the noise signal . . . (figure 5) further see above rational for claim 1.

Regarding claim 20, it is rejected based upon similar rational as claim 11.

Regarding claim 21, Clatanoff discloses the display means is a liquid crystal display (col. 4, lines 40-42)

Regarding claim 22, Clatanoff discloses the image processing apparatus is separately provided. (figures 13 and 14)

Regarding claim 26, Clatanoff discloses the display means is a liquid crystal display (col. 4, lines 40-42)

Regarding claims 27-34, they are rejected based upon similar rational as above claims 1-8 respectively.

Regarding claims 38-42, see above rejection for claims 11-15 respectively.

Regarding claims 43-46, they are rejected based upon similar rational as above claims 1, 2, 6 and 7.

Regarding claims 48-50 and 52-54, they are rejected based upon similar rational as above claims 6-8 respectively.

Regarding claims 56 and 62, they are rejected based upon similar rational as claim 1. Examiner interprets applying gamma correction as a predetermined operation.

Regarding claim 57, Pettitt discloses said first signal processing circuit converts the n-bit digital signal as inputted into the m-bit digital signal according to display characteristics of display means of an image display apparatus provided with said image processing apparatus (col. 3, lines 1-15)

Regarding claim 58, said first signal processing circuit converts the n-bit digital signal as inputted into the m-bit digital signal so as to absorb differences in performances of said driving means for driving display means of an image display apparatus provided with said image processing apparatus (col.

Regarding claim 59, Pettitt discloses said first signal processing circuit converts the n-bit digital signal as inputted into the m-bit digital signal according to ambient brightness of an image display apparatus provided with said image processing apparatus (col. 3, lines 42-50)

Regarding claim 60, see above rejection of claim 59.

Regarding claim 61, Pettitt discloses said first signal processing circuit converts the n-bit digital signal as inputted into the m-bit digital signal according to an average level of an input signal to be inputted to an image display apparatus provided with said image processing apparatus (col. 4, lines 25-32)

Allowable Subject Matter

3. Claims 9, 19, 23-25, 35-37, 41, 51 and 55 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

4. Applicant's arguments with respect to claims 1-62 have been considered but are moot in view of the new ground(s) of rejection.

5. Applicant's arguments, see page 15, filed 04/26/2005, with respect to the rejection(s) of claim(s) 1-8, 10-18, 20-22, 26-34, 38-46, 48-50 and 52-54 under 103 have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new ground(s) of rejection is made in view of Pettitt in view of Clatanoff.

Conclusion

6. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Motilewa A. Good-Johnson whose telephone number is (571) 272-7658. The examiner can normally be reached on Monday, Tuesday and Thursday 9:00 AM - 6:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on (571) 272-3638. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

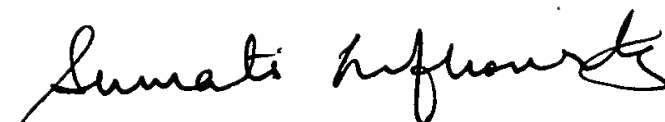
Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Motilewa A. Good-Johnson
Examiner
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